WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Tuesday, January 11, 2005

Hide?	Set Name	Query	Hit Count
		DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
☐	L21	l12 and L20	10
☐	L20	l16 same ((software or program$4) near3 control$7)	32
☐	L19	l12 and l16	429
☐	L18	l12 and L17	1014
☐	L17	L15 and display	18243
☐	L16	L15 same display	7604
☐	L15	((reduc$4 or sav$4) near2 (energy or power) near2 (consum$7 or use or usage))	125538
☐	L14	l3 and L12	0
☐	L13	l1 and L12	4
☐	L12	l8 or l9 or l10 or L11	8544
☐	L11	365/210,226,227,189.09.ccls.	4652
☐	L10	345/98,212.ccls.	1516
☐	L9	713/300,320,321,322,323,324.ccls.	2404
☐	L8	700/21,22.ccls.	141
☐	L7	(profil$4 near3 (display or screen) near3 (use or usage) near3 pattern)	2
☐	L6	(software near3 control$4) same l1	1
☐	L5	l3 and L4	1
☐	L4	(match$4 near3 function$4 near3 (requirement or need))	142
☐	L3	(match$4 near3 energy near3 (requirement or need))	122
☐	L2	L1 same (computer or process$4)	38
☐	L1	energy adj model	175

END OF SEARCH HISTORY

L13: Entry 1 of 4 File: USPT Oct 26, 2004

DOCUMENT-IDENTIFIER: US 6810482 B1
TITLE: System and method for estimating power consumption of a circuit thourgh the use of an energy macro table

Abstract Text (1):
The present invention facilitates relatively accurate power consumption estimates performed at the register transfer level for scaleable circuits with similar architectural characteristics and features. A power evaluation process of the present invention includes a critical path delay based macro energy model creation process and a scaleable power consumption estimation process. In one embodiment of the present invention, the critical path delay based macro energy model creation process provides a base macro energy table and scaling functions (e.g., a bit width scaling function and a normalizing period scaling function). The scaleable power consumption estimation process utilizes the base macro energy table and scaling functions to estimate power consumption of a circuit. The base energy macro table comprises energy values that are based upon a critical path delay period and correspond to normalized toggle rates. Different bit width circuit toggle rates are converted to normalized toggle rates based upon time periods derived from a normalizing period scaling function. The normalized rates are utilized to lookup an energy per event value that is then scaled in accordance with a bit width scaling function of the present invention. The bit width scaling function is a polynomial function based upon a least square error analysis of sample bit width power consumption values corresponding to average characteristic parameters multiplied by a critical path normalization value (e.g., 1.2 times the critical path delay). The scaled energy per event value is divided by the critical path normalization value to provide an power consumption estimate for a particular bit width.

Brief Summary Text (17):
A power evaluation process of the present invention includes a critical path delay based macro energy model creation process and a scaleable power consumption estimation process. In one embodiment of the present invention, the critical path delay based macro energy model creation process provides a base macro energy table and scaling functions (e.g., a bit width scaling function and a normalizing period scaling function). The scaleable power consumption estimation process utilizes the base macro energy table and scaling functions to estimate power consumption of a circuit. The base energy macro table comprises energy values that are based upon normalized toggle rates which are determined by the critical path delay period. Toggle rates for different bit widths are converted to normalized toggle rates based upon time periods derived from a normalizing period scaling function. In one exemplary implementation of the present invention, the normalizing period scaling function is a polynomial function based upon a least square error analysis of critical path normalization values (e.g., 1.2 times the critical path delay) for sample bit widths (e.g., a relatively small selection of possible bit widths). The normalized toggle rates are utilized to lookup an energy per event value that is then scaled in accordance with a bit width scaling function of the present invention. The bit width scaling function is a polynomial function based upon a least square error analysis of sample bit width power consumption values corresponding to average characteristic parameters multiplied by a critical path normalization value (e.g., 1.2 times the critical path delay). The scaled energy per event value is divided by the critical path normalization value to provide an

power consumption estimate for a particular bit width.

Detailed Description Text (5):
Computer system 200 also comprises computer aided design (CAD) tools and performs power evaluation processes of the present invention. Memory components of computer system 200 store present invention power evaluation process information and instructions that are implemented by processor 201. In one exemplary implementation of the present invention, memory 202 stores directions and information associated with critical path delay based macro energy model creation process. Processor 201 performs the critical path delay based macro energy model creation process instructions and computer system 200 stores the results (e.g., a base macro energy table, a bit width scaling function and a normalizing period scaling function stored in memory 202). Computer systems then utilizes these results to estimate power consumption of different bit width circuits based upon a present invention scaleable power consumption estimation process instructions.

Detailed Description Text (6):
FIG. 3 is a flow chart of critical path delay based macro energy model creation method 300. Critical path delay based macro energy model creation method 300 is utilized to characterize a parameterized circuit block such as an adder circuit or multiplier circuit. In one embodiment of the present invention, critical path delay based macro energy model creation method 300 is utilized to estimate power consumption and heat dissipation in symmetrical circuits. For example, critical path delay based macro energy model creation method 300 is utilized in one implementation of the present invention to estimate the power consumption of a 2 by 2 bit width adder circuit, a 4 by 4 bit width adder circuit, a 6 by 6 bit width adder circuit, etc.

Detailed Description Text (15):
In step 420 the normalizing period is calculated using a normalizing period scaling function. In one exemplary implementation of the present invention, the normalizing period scaling function determined in step 330 of critical path delay based macro energy model creation method 300 is utilized.

Detailed Description Text (18):
In step 450 the looked up energy per toggle event is scaled to the value for the desired bit width estimation in accordance with a bit width scaling function of the present invention. In one exemplary implementation of the present invention, the bit width scaling function determined in step 320 of critical path delay based macro energy model creation method 300 is utilized.

Current US Original Classification (1):
713/320

CLAIMS:

1. A critical path delay based macro energy model creation method comprising the steps of: establishing an energy macro table for a particular bit width, said energy macro table including energy per event values based on a critical path delay period; determining bit width scaling functions for scaling energy per event values for different bit-widths; determining a normalizing period scaling function to estimate the normalizing period for the different bit widths; and estimating the power consumption for a particular circuit.

2. The critical path delay based macro energy model creation method of claim 1 in which said energy macro table comprises a three dimensional table.

3. The critical path delay based macro energy model creation method of claim 2 in which said dimensions include a normalized average toggle rate for the inputs (TRin) to a circuit block, an average static probability for the inputs (SPin) of

L13: Entry 4 of 4 File: USPT Sep 17, 1996

DOCUMENT-IDENTIFIER: US 5557557 A
TITLE: Processor power profiler

Abstract Text (1):
A method for determining the energy consumption of a processor when executing a program is provided. The method initially selects the processor which will execute the program and then creates a model of energy used by said processor as a function of a plurality of instructions operable by said processor. The program whose energy consumption is to be determined is then executed using the energy model to determine the energy consumption of the program on the processor.

Brief Summary Text (7):
According to one aspect of the present invention, a power profiler for microprocessors and microcontrollers is provided. In a presently preferred embodiment, a method for determining the energy consumption of a processor when executing a program comprises, selecting the processor which will execute the program, creating a model of energy used by the processor as a function of a plurality of instructions operable by the processor, and determining the energy consumption of the program by executing the program whose energy consumption is to be measured using the energy model.

Detailed Description Text (31):
In summary, a method for determining energy consumption of a processor when executing a program, comprises, selecting a processor, creating a model of energy used by said processor as a function of a plurality of instructions operable by said processor, and executing said program whose energy consumption is to be measured using said energy model to determine said energy consumption of said program.

Current US Cross Reference Classification (3):
713/321

CLAIMS:

5. The method of claim 1, wherein said creating a model step includes attaching said energy model to a simulator for said processor.

6. The method of claim 1, wherein said creating a model step includes attaching said energy model to an emulator for said processor.

L21: Entry 2 of 10 File: USPT Apr 13, 2004

DOCUMENT-IDENTIFIER: US 6721894 B2

**** See image for Certificate of Correction ****

TITLE: METHOD FOR CONTROLLING POWER OF A MICROPROCESSOR BY ASSERTING AND DE-ASSERTING A CONTROL SIGNAL IN RESPONSE CONDITIONS ASSOCIATED WITH THE MICROPROCESSOR ENTERING AND EXITING LOW POWER STATE RESPECTIVELY

Detailed Description Text (4):

The computer system 10 shown in FIG. 1 is a general-purpose architecture common to personal computers such as the IBM Personal Computer and compatibles. The BIOS 16 (basic input/output system) is typically a read-only memory which contains a set of programs for performing the basic control and supervision operations for the computer system 10. The BIOS 16 acts as an interface between the computer circuitry and the application software being executed by the CPU 12. Importantly, for power consumption purposes, the BIOS 16 and logic 18 monitor the circuitry to determine whether power consumption reduction procedures may be invoked. For example, the BIOS 16 and/or logic 18 may monitor the display 34 to determine whether its output has changed over a predetermined time period. If not, the BIOS 16 may invoke procedures to disable power to the display 34 (assuming computer system 10 is a portable computer) to conserve energy. Further, BIOS 16 monitors microprocessor 12 to determine whether the microprocessor can be idled without affecting operation of the computer system 10. For example, the microprocessor 12 may be executing a routine to wait for a character from the keyboard. In this case, the operation of the microprocessor can be suspended until a key is pressed.

Current US Original Classification (1):

713/323

L21: Entry 4 of 10 File: USPT Feb 5, 2002

DOCUMENT-IDENTIFIER: US 6345364 B1
TITLE: Power supply of display apparatus with universal serial bus device

Brief Summary Text (5):
Display apparatus using cathode ray tubes have been used in the personal computer monitors for their high resolution and contrast. Despite technological developments in the display apparatus, the power consumption of the CRT monitor is still considerable. To reduce the monitor power consumption, most computer monitors have power saving function or "green" function as recommended by the Video Electronics Standard Association (VESA). The power saving function of the monitor is performed if there is no input to operate a computer system for a predetermined period of time. Complying with the Display Power Management Signaling (DPMS) scheme established by VESA, the video adapter of the computer system provides the monitor with the horizontal and vertical synchronization signals varied with the power saving modes between full-on, standby, suspend, and power-off state. It automatically reduces the power consumption of the monitor such that an amount of power is decreased with the lapse of time set by the DPMS control program.

Current US Original Classification (1):
713/324

L21: Entry 5 of 10 File: USPT Jan 29, 2002

DOCUMENT-IDENTIFIER: US 6343363 B1
TITLE: Method of invoking a low power mode in a computer system using a halt instruction

Detailed Description Text (4):
The computer system 10 shown in FIG. 1 is a general-purpose architecture common to personal computers such as the IBM Personal Computer and compatibles. The BIOS 16 (basic input/output system) is typically a read-only memory which contains a set of programs for performing the basic control and supervision operations for the computer system 10. The BIOS 16 acts as an interface between the computer circuitry and the application software being executed by the CPU 12. Importantly, for power consumption purposes, the BIOS 16 and logic 18 monitor the circuitry to determine whether power consumption reduction procedures may be invoked. For example, the BIOS.16 and/or logic 18 may monitor the display 34 to determine whether its output has changed over a predetermined time period. If not, the BIOS 16 may invoke procedures to disable power to the display 34 (assuming computer system 10 is a portable computer) to conserve energy. Further, BIOS 16 monitors microprocessor 12 to determine whether the microprocessor can be idled without affecting operation of the computer system 10. For example, the microprocessor 12 may be executing a routine to wait for a character from the keyboard. In this case, the operation of the microprocessor can be suspended until a key is pressed.

Current US Original Classification (1):
713/324

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L21: Entry 6 of 10 File: USPT May 8, 2001

DOCUMENT-IDENTIFIER: US 6230279 B1
TITLE: System and method for dynamically controlling processing speed of a computer in response to user commands

Brief Summary Text (23):
In this computer system, when acceleration or deceleration of the CPU processing speed is instructed by the user through an interface such as a hot key or a button on the display screen, the CPU processing speed is dynamically changed accordingly. The user can therefore dynamically change the current CPU processing speed by manipulating a hot key or button, and can freely change the processing speed in accordance with the contents of a task. This change is recorded as speed management data in correspondence with the name of software such as an application program which has been executed when the processing speed was changed. Every time the user instructs acceleration or deceleration of the CPU processing speed, speed management data is formed. By using the speed management data, the CPU processing speed can be controlled for each piece of software when it is executed. CPU processing speed control can therefore be performed in accordance with a user's intentions such that the CPU processing speed is increased when several specific pieces of software are executed, but decreased for other pieces of software to realize power saving and the like, thus harmonizing the need to reduce the power consumption with the user's wish to obtain a comfortable execution speed.

Current US Original Classification (1):
713/324

Current US Cross Reference Classification (1):
713/322

Previous Doc Next Doc Go to Doc#